REMARKS

Applicant responds hereby to the outstanding Office Action mailed August 2, 2007, in the above-identified application. Claims 1, 10, 11, 14, 15, 17-19 are amended hereby, and claim 12 cancelled without prejudice or disclaimer of subject matter. Each of claims 1-11 and 13-19 remain pending hereinafter, where claims 1, 6, 13 and 16 are the independent claims.

Response To Objection to the Drawings

The drawings were objected to under 37 CFR 1.84(o) for failure to show legends, and failure to fill in the flow charts. In response, applicant provides replacement drawing sheets under 37 CFR 1.121(d), which show legends and filled-in flow-chart elements. In view of the replacement drawing figures, applicant respectfully requests withdrawal of the objection to the drawings

Response To Rejections Under 35 USC §101

Dependent claims 10-12, 14, 15 and 18-19 stand rejected under 35 USC §101 as directed to non-statutory subject matter, i.e., program code. In response, applicant has amended claims 10, 11, 14, 15 and 18-19, and cancelled claim 12 without prejudice or disclaimer of subject matter. Claims 10, 11, 14, 15, 18 and 19 are believed to now comply with Section 101, and applicant, therefore, respectfully requests withdrawal of the rejections.

Response To Rejections Under 35 USC §112

Claims 1-5, 10-12, 14, 15 and 17 stand rejected under 35 USC §112, second paragraph, as indefinite. In response, applicant has amended claims 1, 10, 11, 14, 15 and 17, substantially in

accordance with the Examiner's stated basis for the Second Paragraph rejections. Claims 1-5, 10, 11, 14, 15 and 17 as amended hereby are believed to comply with 35 §112, second paragraph, and applicant respectfully requests withdrawal of the rejection of same claims.

Response To Rejections Under 35 USC §103(a)

Claims 1-19 stand rejected under 35 USC § 103(a) as obvious over US Patent No. 5,473,764 to Chi in view of **1.)** US Patent No. 6,023,726 to Saksena, and **2.)** US Patent No. 5,956.039 to Woods, et al. (Woods).

Claims 1-5

With respect to claim 1, the Examiner asserts that Chi teaches a data packet processing device for processing data packets received from a network, including:

a processor for processing data packets (CPU 10);

an interface (connection 20) operable for transmitting data packets to and from an external memory (main memory 12);

a scheduler for assigning priority information to received data packets (control 24), the priority information determining an order of data packets to be processed;

an internal memory for storing data packets (cache; col. 1, lines 35-50);

a memory manager (control 24) operable to cause storing data packets in the external memory and to provide data packets in the internal memory for being processed by the processor (col. 4, lines 4-15);

wherein the memory manger (control 24) provides data packets in the internal memory (cache, col. 1, lines 35-50) for being processed by the processor subject to the priority information assigned to the data packets (col. 3, lines 4-12; col. 4, lines 50-60).

The Examiner states that Chi is not intended for use in a network environment, but that Saksena teaches cache pre-fetch in a network environment, and that it would have been obvious to modify Chi by the network environment operation of Saksena. With respect to Woods, the Examiner states that Woods teaches cache pre-fetch in a network environment, and that it would have been obvious to modify Chi with Woods to incorporate the Chi system into a network environment operation of Woods.

Applicant has studied Chi, and respectfully disagrees with the Examiner's asserted interpretation of Chi, and the Examiner's conclusion that Chi, when combined with either Saksena or Woods, would have rendered the claim 1 invention been obvious at the time of invention for at least the following reasons.

Chi teaches a cache memory for use by a processor and a main memory that includes a prefetch buffer, a use buffer, and a head buffer. The prefetched buffer is a FIFO or LRU register that prefetches instructions from contiguous memory locations after the address is specified by the program counter. The head buffer is also a FIFO or LRU register for storing instructions from the top of program blocks accessed by main memory following recent cache misses. Chi asserts the shortcomings of prior art cache memories in his Description of the Prior Art at col. 2, lines 20-46.

Chi's cache memory system (Fig. 1) includes a processor 10 and memory 12. Data is transferred between the main memory 12 and processor 10 using a pre-fetch buffer 14, a use buffer 16 and a head buffer 18. Instructions are fetched from the main memory 12 via a system

bus 20 (connection 20) in accord with protocols established by a cache memory control 24. Applicant's understand that the Examiner asserts that Chi's cache memory control is equivalent to applicant's claimed "scheduler for assigning priority information to received data packets, the priority information determining an order of data packets to be processed." Applicants understand by Chi's Fig. 1 and col. 1, lines 35-50, identify that Chi's cache memory embodied in prefetch buffer 14, use buffer 16 and head buffer 18 are what the Examiner asserts to be the equivalent of applicant's "internal memory for storing data packets."

The Examiner asserts that Chi's cache memory control 24 is also equivalent to applicant's "memory manager operable to cause storing data packets in the internal memory for processing by the processor, and that Chi's cache memory control 24 provides data packets to the internal memory (cache buffers 14, 16, 18) processed subject to priority information assigned to the data packets. Applicant easefully disagrees. Applicant's Fig. 1 shows a processor local bus 4 for facilitating communication to/from applicant's claimed memory controller 5 and processor 2, and communicating to/from network 3, and further shows interface 10 for communicating to/from memory controller 5, and to/from external memory 7. Chi's system bus (connection 20 as identified by the Examiner) is shown in Fig. 1 to transfer data from main memory 12 to both the prefetch buffer 14 (internal memory identified by the Examiner) and CPU 10. Chi's connection 20 is not equivalent to applicant's interface operable for transmitting data packets.

While the Examiner asserts that Chi's control 24 is equivalent to applicant's scheduler and memory manager, Chi identifies and describes its control 24 at col. 5, lines 50-54. Chi states that the control unit 24 examines the contents of the three buffers (internal memory, 14, 16, 18) to

determine if the next sequential instruction to be prefetched is already in cache memory. The description does not indicate that control 24 is a scheduler for assigning priority information to received data packets for determining an order of packets to be processed, nor a memory controller operable to cause storing of data packets in external memory and providing data packets in external memory for processing by the processor. Applicants scheduler and memory manager are not equivalent to Chi's control 24, and does not operate as Chi does to identify whether an instruction to be pre-fetched is already in a cache to reduce traffic on system bus 20.

Chi states that its prefetch buffer 14 (internal memory as asserted by the Examiner) is a FIFO used to improve the cache hit ratio by prefetching instructions. Applicant respectfully asserts that it is not an internal memory for storing data packets. Chi states that its head buffer 18 (internal memory as asserted by the Examiner) is a FIFO used to facilitate freezing the first line of a basic block for loop and subroutine instructions improve the cache hit ratio by prefetching instructions. Applicant respectfully asserts that it is not an internal memory for storing data packets. Chi states that its use buffer 14 (internal memory as asserted by the Examiner) is a direct map cache with a large cache size used to reduce traffic on system bus 20. Applicant respectfully asserts that it is not an internal memory for storing data packets.

With respect to the wherein clause in applicant's claim 1, the Examiner asserts that Chi discloses that its Chi's control 24 is equivalent to applicant's claimed memory manager, and provides data packets from internal memory (buffers 14, 16, 18) to be processed by the processor subject to priority information assigned to the data packets. The Examiner explains that where Chi's operation finds no "next" instruction in cache, the control fetches the next instruction from

main memory to the cache. The text at col. 3 refers to head buffer 18, and the text at col. 4 refers to both head buffer 18, use buffer 16. Nowhere does the text refer to priority information assigned to data packets in internal memory, and for processing the data packets.

While the Examiner indicates that Chi may be combined with Saksena, or combined with Woods, to accommodate chi's lack of ability for network operation, applicants do not find that Chi includes each of the elements of applicant's claim 1 as asserted in the outstanding Office Action. Because Chi does not include all of the limitations of applicant's claim 1 but for the network operating ability, applicant respectfully asserts that independent claim 1 is not obvious over Chi combined with 1.) Saksena, nor 2.) Woods, under Section 103(a), and respectfully requests withdrawal of the Section 103(a) rejections.

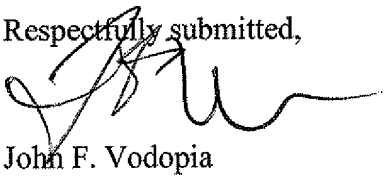
Claims 6-19

With respect to claims 6-19, the Examiner asserts that these claims have similar limitations as claims 1-5, and are rejected for the same reasons.

In response, applicant respectfully asserts that claims 6-19 are patentable under Section 103(a) over Chi in view of **1.)** Saksena and **2.)** Woods for at least the same reasons set forth above for the patentability of claims 1, and 2-5, and requests withdrawal of same Section 103(a) rejections.

If the Examiner believes that a telephone conference with applicant's attorneys would be advantageous to the disposition of this case, the Examiner is asked to telephone the undersigned.

Respectfully submitted,



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